UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/605,418 | 09/30/2003 | Yao-Huang Hsieh | MTKP0093USA | 2417 |

27765 7590 03/12/2007

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

| EXAMINER | |
|---|---|
| VICARY, KEITH E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | NOTIFICATION DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/12/2007 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/12/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,418 | HSIEH, YAO-HUANG | |
| | Examiner | Art Unit | |
| | Keith Vicary | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-5 are pending in this application and presented for examination.

### *Specification*

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

a. Throughout the application, there are words that are not separated by spaces, such as in [0002], line 1, "systemfor," or [0017], lines 2-3 "comprisesa." Furthermore, there are other typos such as two consecutive commas in [0013], line 11. This is not intended to be an exhaustive list of all typos in the specification; these typos must be fixed.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Objections*

4. Claims 1-3 are objected to because of the following informalities. Appropriate correction is required.

b. "afirst," claim 1, should be "a first."

c. "aninitializing," claim 1, should be "an initializing."

d. "storingthe," claim 2, should be "storing the."

e. "comparinga," claim 3, should be "comparing a."

f. "anintializing," claim 3, should be "an initializing."

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 3 recites the limitation "the table entry" in the last line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this office action, the examiner is reading the limitation to read "an entry of the table."

g. Claims 4 and 5 are rejected for failing to alleviate the rejections of claim 3 above.

8. Claim 4 recites the limitation "the patch" in line 2. There is insufficient antecedent basis for this limitation in the claim, as this limitation may differ from "patch program segments" of claim 3, line 1.

h. Claim 5 is rejected for failing to alleviate the rejection of claim 4 above.

9. Claim 5 recites the limitation "the read only memory" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

10. In claim 1, the applicant should insert indentations and lines between the paragraphs designating the components of the apparatus in order to better convey the components of this apparatus. It is indefinite as to where in the apparatus the read only

memory, the auxiliary programmable-memory, and the controller lie. For example, it is unclear as to whether a read only memory is part of solely the microprocessor apparatus, the microprocessor apparatus and the processing unit, or the microprocessor apparatus, the processing unit, and the instruction decoding means.

i. Claim 2 is rejected for failing to alleviate the rejection of claim 1 above.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagqvist et al. (Hagqvist) (US 5581776).

13. **Consider claim 1**, Hagqvist discloses a microprocessor apparatus comprising: a program counter for storing a program count value (Figure 1, program counter 28); a processing unit coupled to the program counter comprising: an instruction fetching means coupled to the program counter for reading program instructions according to the program count value and storing fetched instructions in a buffer (col. 1, lines 17-19, program counter output causes an instruction fetch from the program; it is inherent that any fetched instructions are placed in some form of buffer); an instruction decoding means coupled to the instruction fetching means for decoding and dispatching buffered instructions for execution (it is inherent in a microprocessor that fetched instructions are

subsequently decoded and dispatched for execution; otherwise, the program would never actually run); a read only memory coupled to the processing unit for storing a first program (Figure 1, ROM 14 and operating program 15); an auxiliary programmable memory coupled to the processing unit for storing patches to replace corresponding instructions in the first program (Figure 1, ROM/RAM 20, and col. 2, lines 21-24, which shows that it stores code that is to be substituted for code of operating program 15) along with a table containing a replacement program count value for each patch (the memory of ROM/RAM 20 itself is the table, and the replacement program count value is analogous to a memory address; just as a memory contains addresses at which data is stored, so to does the ROM/RAM contain replacement program count values at which replacement instructions are stored); and a controller coupled to the program counter and the processing unit for passing an indirect branch instruction corresponding to one of the patches to the processing unit (Figure 1, program counter load controller 26, col. 2, line 67 and col. 3, lines 1-2 show the program counter load controller loading a value in the branch control register into the program counter, and col. 2, lines 38-40 show that the branch control register stores the address of the alternate program; this replacement of the program counter constitutes an indirect branch instruction, as the microprocessor is indirectly instructed to branch without a branch instruction actually being decoded) in response to a match between the program count value and an initializing program count value (col. 2, lines 64-67, program count output matches the pre-loaded address value of col. 2, lines 56-58, which define the count at which a branch action is to commence), wherein the indirect branch instruction will insert the

replacement program count value corresponding to the match into the program counter (col. 2, line 67 and col. 3, lines 1-2, program counter load controller causes the value stored in branch control register to be loaded into program counter).

14. **Consider claim 2**, Hagqvist discloses a register for storing the initializing program count value (Figure 1, address comparator 22, which is shown in col. 2, lines 56-58, to have registers loaded with address values which define the count at which a branch action is to commence).

15. **Consider claim 3**, Hagqvist discloses a method for executing patch program segments in lieu of corresponding parts in a first program comprising: (a) comparing a program count value of a program counter with an initializing program count value (col. 2, lines 64-67, program output matches the preloaded address value of col. 2, lines 56-58, which define the count at which a branch action is to commence); (b) inserting an indirect branch instruction with an index into a buffer of an instruction fetching means when a match is made in step (a) (col. 2, line 67 and col. 3, lines 1-8, when the program counter output matches the pre-loaded address value, as above, program counter load controller causes the value stored in branch control register to be loaded into program counter; this replacement of the program counter constitutes an indirect branch instruction, as the microprocessor is indirectly instructed to branch without a branch instruction actually being decoded. The index of this branch instruction is the replacement program counter, and the index is inserted into the ROM/RAM auxiliary

memory, which correlates to a buffer of an instruction fetching means) (c) accessing a table in an auxiliary programmable memory according to the index of the indirect branch instruction (Figure 1, ROM/RAM 20 serves as the auxiliary memory and the table, and col. 3, lines 35-38 discloses responding to program count by accessing the address in auxiliary storage module; given that the index of the indirect branch instruction was the value of the replacement program counter as explained above, it is clear that the table in memory is accessed via the replacement program counter which serves as an index into the table); and (d) changing the program count value of the program counter according to the table entry (col. 3, lines 32-35; program count written from branch control register into program counter; the new program counter value is in accordance with the address of the table entry that should be executed next, due to the encountering of the initializing program counter value of col. 2, lines 56-58. Alternatively, the replacement instruction in the addressed table entry may be a jump instruction or a non-jump instruction; based on which one it is, the next program counter will be updated accordingly).

16. **Consider claim 4**, Hagqvist discloses ending the patch with a terminating instruction branch (col. 3, lines 18-21, "branch-to" instruction, which causes a return to the main program).

17. **Consider claim 5**, Hagqvist discloses branching back to the first program in the read only memory with the terminating branch instruction (col. 3, lines 18-21, "branch-to" instruction, which causes a return to the main program).

***Conclusion***

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KV

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100